Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	(logic near gate) and stack and region and (substrate or wafer or semiconductor) and (flash near memory) and (deposit near8 hardmask) and pattern$4 and etch$4 and die and dielectric and electrode and float$4 and control and (ARC or "anti-rflective coating") and pitch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:27
S2	0	logic and stack and region and (substrate or wafer or semiconductor) and (flash near memory) and (deposit near8 hardmask) and pattern$4 and etch$4 and die and dielectric and electrode and float$4 and control and (ARC or "anti-rflective coating") and pitch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:27
S3	0	logic and stack and region and (substrate or wafer or semiconductor) and (flash near memory) and (deposit near8 hardmask) and pattern$4 and etch$4 and die and dielectric and electrode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:27
S4	0	logic and stack and region and (substrate or wafer or semiconductor) and (flash near memory) and (deposit near8 hardmask) and pattern$4 and etch$4 and die	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:27
S5	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and (deposit near8 hardmask) and pattern$4 and etch$4 and die	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:28
S6	26	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:28
S7	23	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:28

S8	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode and (ARC or "anti-reflective coating")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:29
S9	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode and (ARC or "anti reflective coating")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:29
S10	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode and ARC	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:29
S11	0	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode and reflective	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:29
S12	23	logic and stack and region and (substrate or wafer or semiconductor) and flash and memory and deposit and hardmask and pattern$4 and etch$4 and die and dielectric and electrode	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:00
S13	38	flash adj logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:01
S14	1	flash adj logic and hardmask and pattern$4 and etch$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:02

S15	1	flash adj logic and hardmask	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:02
S16	6	flash adj logic and (ARC or "anti-reflective coat$4")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:03
S17	3	flash adj logic and (ARC or "anti-reflective coat$4") and pattern	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:03
S18	3	flash adj logic and (ARC or "anti-reflective coat$4") and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 11:03
S19	3	flash adj logic and (ARC or "anti-reflective coat$4") and pattern and etch and (substrate or semicondcutor or wafer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 12:41
S20	3	flash adj logic and (ARC or "anti-reflective coat$4") and pattern and etch and (substrate or semicondcutor or wafer) and resist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 12:48
S21	0	flash adj logic and (ARC or "anti-reflective coat$4") and pattern and etch and (substrate or semicondcutor or wafer) and resist and float	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 13:00
S22	12	logic and flash and substrate and memory and "ARC" and (resist near4 resist) and pattern and etch	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 12:50